ABSTRACT OF THE DISCLOSURE

An apparatus comprising a clock generation circuit, a detect circuit and a select circuit. The clock generator circuit may be configured to generate an output clock signal in response to a control signal. The detect circuit may be configured to generate a detect signal in response to (i) the output clock signal and (ii) an input signal. The select circuit may be configured to generate the control signal by selecting (i) a first input when in a first mode (ii) the detect signal when in a second mode. The first and second modes are selected in response to a selection signal.